

Application No. 09/527,761
Amendment dated October 6, 2005
Reply to Office Action of July 7, 2005

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS

1. (Currently Amended) A semiconductor wafer, comprising:
a plurality of pits in the semiconductor wafer, the pits being arranged in a digital information-providing pattern,
a coating of sapphire or silicon carbide on a surface of each of the plurality of pits,
said digital information-providing pattern being arranged in a pattern other than a bar code pattern,
said digital information-providing pattern being arranged and suitably adapted to be readable before, during and after completion of processing on the wafer.
2. (Previously Presented) The wafer according to claim 1, wherein a readability of the pits is provided by the pits having a detectable contrast with respect to surrounding portions of the wafer.
3. (Previously Presented) The wafer according to claim 2, wherein the pits are arranged in a region of the wafer, wherein the contrast is provided by an ion implant in the region.
4. (Previously Presented) The wafer according to claim 3, wherein the ion implant is carried out to an implant depth and the pits have a pit depth greater than the implant depth.

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5. (Previously Presented) The wafer according to claim 2, wherein the pits are arranged in a region of the wafer, wherein the detectable contrast is provided by a depth of the pits.

6. (Previously Presented) The wafer according to claim 1, wherein the digital information providing-pattern comprises at least one of a binary pattern and an alphanumeric pattern.

7. (Previously Presented) The wafer according to claim 1, wherein the digital pattern comprises long and short pits.

8. (Original) The wafer according to claim 1, wherein the plurality of pits comprise pits of a first shape and pits of a second shape.

9. (Original) The wafer according to claim 1, wherein the pits are on at least one surface of the wafer selected from the group consisting of a front surface, a back surface, and a side surface.

10. (Original) The wafer according to claim 1, wherein the pits are at least 2.5 μm deep.

11. (Original) The wafer according to claim 1, wherein the pits are on a side surface of the wafer extending from a front surface of the wafer to a back surface of the wafer.

12. (Original) The wafer according to claim 11, wherein the pits on the side surface of the wafer are formed prior to slicing the wafer from a boule by providing diagonal lines in the boule to provide a unique pattern on each wafer sliced from the boule.

13. (Original) The wafer according to claim 1, wherein the pits are readable by a reader's eye.

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14. (Original) The wafer according to claim 1, wherein the pits are readable with a laser reading device.
15. (Canceled)
16. (Previously Presented) The wafer according to claim 1, wherein the pits have a width of at most approximately 1 mm and a depth of at most approximately 1 mm.
17. (Original) The wafer according to claim 1, wherein a bottom surface of the pits is curved.
18. (Original) The wafer according to claim 1, wherein at least one of the pits is perpendicular to a top surface and a bottom surface of the wafer.
19. (Original) The wafer according to claim 1, wherein at least one of the pits is angled with respect to a line perpendicular to a top surface and a bottom surface of the wafer.
20. (Original) The wafer according to claim 1, wherein at least one of the pits has curved sidewalls.
21. (Original) The wafer according to claim 1, wherein the pits have at least two different widths.
22. (Original) The wafer according to claim 1, wherein the pits are machine-readable.
23. (Original) The wafer according to claim 8, wherein the pits are arranged in the back surface of the wafer.
24. (Original) The wafer according to claim 23, wherein groups of the pits have the shape of at least one of letters and numbers.
25. (Previously Presented) The wafer according to claim 24, wherein each group of pits has a width of approximately 2 mm and a height of approximately 5 mm.

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26. (Previously Presented) The wafer according to claim 24, wherein adjacent groups of pits are separated from each other by a distance of approximately 2 mm.

27. (Currently Amended) A semiconductor wafer, comprising:
a plurality of pits in the semiconductor wafer, the pits being arranged in a digital
information-providing pattern,
said digital information-providing pattern being arranged in a pattern other than a bar
code pattern,
said digital information-providing pattern being arranged and suitably adapted to be
readable before, during and after completion of processing on the wafer,
wherein the plurality of pits comprise pits of a first shape and pits of a second shape,
wherein the pits are arranged in the back surface of the wafer,
wherein groups of the pits have the shape of at least one of letters and numbers,

The wafer according to claim 24, wherein each group of pits includes a machine-readable
set of spaces for pits, each space comprising 2 columns each comprising 32 pits.

28. (Original) The wafer according to claim 1, wherein light striking spaces between the pits form interference fringes.

29. (Original) The wafer according to claim 1, wherein light striking the pits is not reflected.

30. (Original) The wafer according to claim 1, wherein light striking the pits is reflected with a phase change.

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31. (Original) The wafer according to claim 1, wherein the pits comprise at least one location pit for providing locational reference to a plurality of informational pits.

32. (Original) The wafer according to claim 31, wherein the location pit is arranged in a side edge of the wafer and the informational pits are located in a top surface or a bottom surface of the wafer.

33. (Original) The wafer according to claim 1, wherein the pits have the same widths and at least two different lengths.

34. (Original) The wafer according to claim 33, wherein the pits are arranged in at least one line.

35. (Previously Presented) The wafer according to claim 33, wherein adjacent pits in a line or in adjacent lines are separated by a distance of at least 5 μm .

36. (Original) The wafer according to claim 15, wherein the coating is sapphire or silicon carbide.

37. (Currently Amended) A method of encoding information on a semiconductor wafer, comprising:

converting the information into a digital form,

said digital form being a form other than a bar code pattern; and

forming pits suitable for being read before, during and after completion of processing on the wafer corresponding to the digital form of the information in the semiconductor wafer,

wherein said pits are formed before processing of the wafer begins, during wafer processing, or after wafer processing is completed.

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wherein said pits are formed during wafer processing to record information about the processing.

38. (Original) The method according to claim 37, wherein forming the pits comprises: forming a line of pits having two different lengths, the line of pits corresponding to the digital form of the information.

39. (Original) The method according to claim 37, further comprising:
forming a reference point, such that the pits are located a predetermined distance from the reference point.

40. (Original) The method according to claim 37, further comprising:
providing the pits with a detectable contrast with respect to surrounding portions of the wafer.

41. (Original) The method according to claim 37, wherein the pits are formed prior to cutting the wafer from a boule and forming the pits comprises:

forming a first, curved groove in the boule;

forming at least one linear groove in the boule; and

slicing the boule into wafers.

42. (Original) The method according to claim 37, further comprising: coating the pits with a coating.

43. (Original) The method according to claim 37, further comprising: reading the information represented by the pits.

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44. (Original) The method according to claim 43, wherein the information is read with a machine.

45. (Original) The method according to claim 43, wherein the information is readable by an unaided human eye.

46. (Canceled)

47. (Canceled)

48. (Currently Amended) The method according to claim 4637, wherein pits previously formed are altered.

49. (Currently Amended) The method according to claim 4637, further comprising the step of reading pits formed during processing and using the information read to determine a subsequent process parameter.

50. (Original) The method according to claim 37, wherein pits previously formed are invalidated.

51. (Canceled)

52. (Canceled)

53. (Canceled)

54. (Canceled)

55. (Previously Presented) The semiconductor wafer according to claim 1, wherein the plurality of pits are simultaneously arranged in both the digital information-providing pattern and a human-readable pattern.

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56. (Previously Presented) The semiconductor wafer according to claim 1, wherein the digital information-providing pattern is a non-binary coded pattern, and the plurality of pits comprise pits having at least three different shapes.

57. (Canceled)

58. (Previously Presented) The semiconductor wafer according to claim 1, wherein the digital information-providing pattern is a non-binary coded pattern, and the plurality of pits comprise a plurality of differently oriented oval pits as defined by an orientation of each of an associated major axis thereof.

59. (Previously Presented) The semiconductor wafer according to claim 58, wherein the non-binary coded pattern is a quaternary-coded pattern.

60. (Previously Presented) The method of claim 37, further comprising simultaneously arranging the pits to correspond both to the digital form and to a human-readable pattern.

61. (Previously Presented) The system of claim 37, wherein said step of forming pits includes forming pits having at least three different shapes.

62. (Canceled)

63. (Previously Presented) The system of claim 37, wherein said step of converting the information into the digital form includes converting the information into a non-binary digital form, and said step of forming pits includes forming pits in a plurality of differently oriented oval pits as defined by an orientation of each of an associated major axis thereof.

64. (Canceled)

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65. (Previously Presented) The method of claim 37, further comprising scribing linear wafer sequence start notch along a longitudinal surface of a boule from which a plurality of semiconductor wafers are subsequently encoded and cut.

66. (Previously Presented) The method of claim 65, further comprising scribing a plurality of essentially helically-shaped boule sequence notches along the longitudinal surface.

67. (Previously Presented) The method of claim 37, further comprising scribing a plurality of essentially helically-shaped boule sequence notches along a longitudinal surface of a boule from which a plurality of semiconductor wafers are subsequently encoded and cut.